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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,523	12/31/2003	Kimming So	15057US02	1971

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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/750,523	Applicant(s) SO ET AL.	
	Examiner Yaima Campos	Art Unit 2185	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 15 December 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-20.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

Continuation of 11. does NOT place the application in condition for allowance because: 1st POINT OF ARGUMENT

1. In response to Applicant's arguments, the recitation "A method of reducing the size of a translation lookaside buffer comprising" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

2ND POINT OF ARGUMENT

2. Regarding Applicant's remark that Hinton does not disclose "utilizing a bit obtained from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of said translation lookaside buffer" of a translation lookaside buffer; the Examiner disagrees and provides the following explanation:

As per Applicant's argument that Hinton does not disclose a "virtual page number;" [Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Applicant's claimed page number]

As per the limitation "utilizing a bit obtained from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of said translation lookaside buffer" [Hinton discloses "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3]. For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant. Applicant is reminded that the claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

3RD POINT OF ARGUMENT

3. Regarding Applicant's remark that Hinton does not utilize a bit that corresponds to a least significant bit of a virtual page number; the Examiner maintains her position. [Applicant's Specification defines a least significant bit as "a least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described)" (Page 3, Paragraph 0026) and Hinton discloses "a logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page... bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB" (Col. 6, lines 38-43) which clearly corresponds to bit 12 (which is defined as the least significant bit of a virtual page number) of a 32-bit logical address, as defined by Applicant]. Furthermore; it is the Examiner's position that to one of ordinary skill in the art, the position of the "bit obtained from a virtual page number for the purposes of writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer is a matter of design choice as it appears that the invention would perform equally well with (the least significant bit or any other bit within a virtual page number selected to serve the same purpose as disclosed by Hinton and claimed by Applicant).

4TH POINT OF ARGUMENT

4. Regarding Applicant's remark that Hinton's invention uses two buffers (i.e., a TLB and a TWB) compared to Applicant's invention that recites a single buffer; it is the Examiner's position that Hinton discloses all the limitations required by the claimed language. The TWB recited by Hinton corresponds to Applicant's claimed TLB (Translation Lookaside Buffer). Applicant should note (1st Point of Argument above).

5TH POINT OF ARGUMENT

5. In response to Applicant's argument challenging the rejection to claims 3, 5, 10, 14, 20 and 4, 11; the Examiner maintains her position as it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use an existing translation lookaside buffer control instruction set and make the translation lookaside buffer as taught by Hinton compatible with existing TLB instructions, software, or commands as one of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing components. The examiner has provided a motivation one of ordinary skill would have had to make an invention compatible with existing TLB instructions, software, or commands. Furthermore, as the claims recite "existing translation lookaside (TLB) control processor instruction set;" the claims are recognizing these existing TLB instruction sets as being "older;" therefore, comprising prior art; including MIPS processor instruction set.

6TH POINT OF ARGUMENT

6. In response to Applicant's remarks that it would not have been obvious to combine Hinton and Kirk as the references are nonanalogous art, it has been held that a prior art reference must either be in the field of Applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the Applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, both Hinton and Kirk involve in virtual to physical address translation using a TLB. Furthermore, the reference to Kirk has merely been provided to illustrate that MIPS (Millions Instructions Per Second) processor instruction set is well-known in art at the time of the invention; therefore, comprising prior art.

7TH POINT OF ARGUMENT

7. In response to Applicant's remark challenging the rejection to claim 7, the examiner maintains her position [Refer to rejection to claim 7]. Furthermore, one of ordinary skill in the art would recognize, the position of the "virtual page number" within a 32-bit virtual address is a matter of design choice as it appears that the invention would perform equally well with the virtual page number defined as bits [13-31] as taught by Hinton or bits [31:12] as claimed by Applicant. The reference to Bryg has been provided as proof that the positions of a virtual page number are system-specific; therefore, each inventor may choose where to place a virtual page number within a virtual address.

8TH POINT OF ARGUMENT

8. In response to Applicant's argument that there is not suggestion to combine the references to Hinton and Bryg, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Hinton and Bryg are directed to and involved in virtual address translation.

9TH POINT OF ARGUMENT

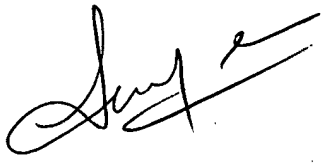
9. Regarding Applicant's remark with respect to the rejection of claims 8-9 which recite "wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes" or "wherein said page mask size comprises 4 kilobytes;" the Examiner maintains her position that it would have been obvious to one of ordinary skill in the art to [use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping] as the size of a page mask is a matter of design choice as it appears that the invention would perform equally well with any size of page mask. The reference to Riedlinger has been provided as proof that it is well known in the art at time of the invention that the page mask size is used to selected a virtual page size.

Regarding applicant's argument that "the page mask size as used in the various aspects of Applicant's claimed invention provides a preferred embodiment (i.e., a preferred range) in which the claimed invention may be realized;" Applicant should note that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Furthermore, the recitations of "wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes" or "wherein said page mask size comprises 4 kilobytes;" is a mere change in size of a virtual page mask size. A change is size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

10TH POINT OF ARGUMENT

10. In response to Applicant's argument that there is not suggestion to combine the references to Hinton and Riedlinger, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Hinton and Riedlinger are directed to and involved in virtual address translation.



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